This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1. (Previously presented) A thin film transistor array panel comprising:

an insulating substrate;

a gate wire formed on the substrate and including a plurality of gate lines and a plurality of gate electrodes connected to the gate lines;

a gate insulating layer formed on the gate line;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the semiconductor layer and including a plurality of data lines intersecting the gate lines, a plurality of source electrodes connected to the data lines, and a plurality of drain electrodes located opposite the source electrodes with respect to the gate electrodes;

a plurality of pixel electrodes connected to the drain electrodes; and

an etching assistant pattern made of the same layer as the semiconductor layer and located out of an area enclosed by the gate lines and the data lines.

2. (Original) The thin film transistor array panel of claim 1, wherein the data wire comprises a lower film of Cr, Mo or Mo ally and an upper film of Al or Al ally.

3. (Original) The thin film transistor array panel of claim 2, further comprising a passivation layer disposed between the data wire and the pixel electrode.

4. (Original) The thin film transistor array panel of claim 3, wherein the semiconductor layer has substantially the same planar shape as the data wire except for a channel portion located between the data line and the drain electrode.

5. (Withdrawn) A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate wire including a gate line and a gate electrode on a substrate;

forming a gate insulating layer on the substrate;

forming a semiconductor pattern and an etching assistant pattern on the gate insulating layer;

forming a source/drain conductor pattern and an etching assistant layer on the semiconductor pattern and the etching assistant pattern;

forming a data wire including a data line and source and drain electrodes separated from each other by removing the etching assistant layer and partly removing the source/drain conductor pattern; and

forming a pixel electrode connected to the drain electrodes.

6. (Withdrawn) The method of claim 5, wherein the separation of the source and the drain electrodes are performed by using a photo-etching process using a photoresist pattern, and the photoresist pattern comprises a first portion disposed on an etching assistant portion and having a first thickness, a second portion having a second thickness larger than the first thickness, and a third portion disposed at positions except for the first and the second portions and having a thickness smaller than the first thickness.

7. (Withdrawn) The method of claim 6, wherein a mask used for the photo-etching process comprises a first portion partly transmitting light, a second portion fully transmitting light, and a third portion fully blocking light, and the first, the second and the third portions of the mask is aligned to face the first, the second and the third portions of the photoresist pattern, respectively, during light exposure.

8. (Withdrawn) The method of claim 6, further comprising: forming a contact pattern between the data wire and the semiconductor pattern, wherein the data wire, the contact pattern, the semiconductor pattern, and the etching assistant pattern are formed by using a mask.

9. (Withdrawn) The method of claim 8, wherein the formation of the gate insulating layer, the semiconductor pattern, the contact pattern, and the data wire comprises:

depositing the gate insulating layer, a semiconductor layer, a contact layer, and a conductive layer;

coating a photoresist film on the conductive layer;

exposing the photoresist film through the mask;

developing the photoresist film to form the photoresist pattern such that the second portion of the photoresist pattern is disposed on the data wire;

forming the data wire, the contact pattern, and the semiconductor pattern respectively made of the conductive layer, the contact layer and the semiconductor layer by removing a portion of the conductive layer under the third portion, the semiconductor layer and the contact layer thereunder, the first portion, the conductive layer and the ohmic contact layer under the first portion, and a partial thickness of the second portion; and removing the photoresist pattern.

10. (Withdrawn) The method of claim 9, wherein the formation of the data wire, the contact pattern, the semiconductor pattern, and the etching assistant pattern comprises:

removing the portion of the conductive layer under the third portion by dry etching or wet etching to form the source/drain conductor pattern and the etching assistant layer;

etching the contact layer under the third portion, the semiconductor layer thereunder to complete the semiconductor pattern and the etching assistant pattern under the first and the second portions; and

removing the source/drain conductor pattern and the etching assistant layer to complete the data wire and the contact pattern.

11. (Withdrawn) The method of claim 10; wherein the data wire comprises a lower film including Cr, Mo or Mo alloy and an upper film including Al or Al alloy.

12. (Withdrawn) The method of claim 11, wherein the upper film and the lower film are patterned by wet etching.

13. (Previously presented) The thin film transistor array panel of claim 1, wherein the etching assistant pattern is located outside of a pixel area.

14. (Previously presented) The thin film transistor array panel of claim 1, wherein the etching assistant pattern is formed directly on the gate insulating layer.

15. (Previously presented) The thin film transistor array panel of claim 1, wherein the thickness of the etching assistant pattern is thinner than a thickness of the semiconductor layer